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Int. Cl.:—H 03 k 17/04 // H02j, m.

COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Transistor Switching Circuit

We, GENERAL ELECTRIC COMPANY, a corporation organised and existing under the laws of the State of New York, United States of America, of 1 River Road, Schenectady 5, New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a transistor switching circuit and finds particular application in high frequency chopper circuits for use in inverters and time ratio control power circuits.

With the advent of power semiconductor devices for switching electric currents at power levels, such as the silicon controlled rectifier (SCR) and the power transistor, there has been a continuing effort to employ such devices for switching purposes at higher and higher frequencies. To accomplish this, the present invention employs a tunnel diode in conjunction with a transistor to achieve high speed switching of the transistor. As a consequence, circuits employing the invention may be operated at higher chopping frequencies than heretofore possible.

According to the invention, there is provided a switching circuit comprising a transistor; a tunnel diode connected between the emitter and base of the transistor with like polarity to the emitter-base junction; and a saturable transformer having a first winding and a second winding which is coupled to the base and emitter of the transistor to apply switching signals thereto.

This invention will be better understood by reference to the following detailed description, when considered in connection with the accompanying drawings, wherein like parts in each of the several figures are identified by

the same reference character, and wherein:

FIGURE 1 is a schematic equivalent circuit diagram of a tunnel diode, power transistor switching circuit arrangement in accordance with the invention, together with a series of characteristic curves illustrating the manner of operation of the arrangement;

FIGURE 2 is a pair of voltage versus current characteristic curves for the circuit arrangement of FIGURE 1;

FIGURE 3 is the equivalent circuit of a modified form of a tunnel diode-power transistor switching circuit arrangement constructed in accordance with the invention;

FIGURE 4 is a schematic circuit diagram of one preferred form of high frequency chopping circuit constructed in accordance with the invention;

FIGURE 5 is an equivalent circuit diagram of the preferred high frequency chopping circuit arrangement of FIGURE 4 illustrating the impedances and voltages which affect operation of the circuit;

FIGURE 6 is a schematic circuit diagram for illustrating the principles of a particular manner of controlling a high frequency, chopping circuit.

FIGURE 7 is a series of current versus time characteristic curves illustrating the mode of operation of the circuit of FIGURE 6;

FIGURE 8 is a schematic circuit diagram of a high frequency chopping circuit according to the invention and employing the principles enumerated with respect to the circuit arrangement of FIGURE 6;

FIGURE 9 is a detailed circuit diagram of one half of a bridge power inverter circuit, and illustrates the use of the high frequency chopping circuit arrangement of the present invention to control operation of the bridge power inverter; and

FIGURE 10 is a simplified schematic circuit diagram illustrating the manner of connection of the power transistors in the bridge power inverter of which a detailed portion is shown in Figure 9.

In the circuit arrangement of FIGURE 1, a battery 31 and switch 32 are used to depict the switching saturable core transformer employed since these elements will perform equivalent circuit function of the saturable core transformer. As shown in FIGURE 1, the battery 31 and switch 32 are connected across the emitter-base of the power transistor 11. In addition, a tunnel diode 33 is connected across the emitter-base junction of the power transistor 11 with like polarity to the junction, that is with the anode 34 of the tunnel diode being connected to the emitter of transistor 11 and the cathode 35 of the tunnel diode being connected to the base of power transistor 11. The resistance of the leads and conductors interconnecting these elements is shown at 36 and the distributed inductance of the leads is illustrated at 37 since each of these values will affect operation of the circuit.

The wave forms shown in FIGURES 1b through 1d of the drawings considered in conjunction with FIGURE 2 of the drawings illustrates the manner of operation of the tunnel diode 33 to achieve very fast switching of the base current of the power transistor 11. If at time zero in FIGURE 1b the switch 32 is closed, the rise in current i_{on} flowing through the circuit of FIGURE 1 would be as shown in FIGURE 1b. This current would cause a small current i_b to flow in the emitter-base circuit of power transistor 11 as well as a current i_t flowing through the tunnel diode 33. As shown in FIGURE 2 of the drawings, the current through the tunnel diode i_t will initially greatly exceed the base current as can be appreciated by comparing the values of the two currents at a point in time marked a in FIGURE 2. Upon the current through the tunnel diode 33 reaching the value indicated at point a in FIGURE 2 after about 1-5 microseconds, the voltage across the tunnel diode will suddenly shift to its higher value indicated at point a_1 due to the well known tunneling characteristic of the tunnel diode. This shift to a higher voltage is accomplished practically instantaneously so that it can be appreciated that the emitter-base of the power transistor 11 is subjected to an instantaneous increase in potential across it. This results in a sudden rise in current through the emitter-base of the power transistor 11 as depicted by the dotted line in FIGURE 2. The time for the sudden rise in current through the emitter base of the power transistor 11, and consequently the time in which it is switched to its full on condition, is very short, less than .02 microseconds. Subsequently, the current

through the tunnel diode will drop from the position shown at point a_1 to the position shown at point b at the same time that the current through the emitter-base of the power transistor 11 rises to the point b shown in FIGURE 2. Thereafter the current through each of the devices shifts to the point c as the current continues to rise through the circuit until it reaches its steady state value determined by the value of the parameters 36 and 37 as well as the voltage of the source 31. The current through the tunnel diode i_t is illustrated by the curve shown in FIGURE 1c of the drawings wherein it can be seen that the current i_t rises until it reaches the point a and then immediately drops to its lower value as the tunnel diode shifts to its higher voltage mode of operation. Concurrently, the base current i_b flowing in the emitter-base of the power transistor 11 increases very slowly until the time that the current through tunnel diode reaches the point a and the tunnel diode shifts to its higher voltage mode of operation, then the current i_b rises almost instantaneously to almost its ultimate limiting value. The tunnel diode and base-emitter characteristic illustrated in FIGURES 1 and 2 are shown for a germanium power transistor unit such as the 2N1907, and for a pair of parallel-connected germanium tunnel diodes, such as the GE 1N3851 connected in parallel with a 1N3850. If silicon power transistors are preferred, then a silicon tunnel diode such as the 1N2933 and 1N2934 could be used in place of those illustrated. The combination of germanium power transistors together with germanium tunnel diodes is preferred, however, since the germanium power transistors have a lower base-emitter voltage drop when turned on (hence less power loss) and they cost less than the silicon power transistors. The silicon power transistors, however, may be preferred for high temperature applications.

The use of a tunnel diode 33 to accomplish fast turn on of the power transistor 11 as explained in connection with FIGURES 1 and 2 is quite effective. However, the tunnel diode by its presence alone can prevent fast turn off of power transistor 11. Since in order to accomplish high frequency chopping, it is imperative that the transistor not only be turned on fast, but that it also be turned off fast to achieve the desired end. To accomplish this, the circuit modifications shown in FIGURE 3 are included. In the circuit arrangement shown in FIGURE 3, a blocking diode is connected in series circuit relationship with the tunnel diode 33 in a manner such that current flows through both the tunnel diode and blocking diode 41 in the same direction. The series circuit comprised by tunnel diode 33 and blocking diode 41 is connected across the emitter-base of the

power transistor 11, and a source of reverse bias voltage 42 and series connected switch 43 likewise are connected across the emitter-base of power transistor 11. Because the inclusion of the blocking diode 41 may cause a mismatch in the impedance between the tunnel diode 33 and the emitter-base of power transistor 11, an impedance matching diode 44 (or diodes) is connected in series circuit relationship with the emitter-base of power transistor 11. The series circuit comprised by the tunnel diode 33 and blocking diode 41 is then connected in parallel circuit relationship with the series circuit comprised by the impedance matching diode 44 and the emitter-base of power transistor 11. By this arrangement, when the switch 43 is closed and the switch 32 concurrently opened, a reverse bias potential will be applied across the emitter-base of power transistor 11, thereby causing it to quickly turn off since the reverse bias potential from the source 42 will be blocked by blocking diode 41. The added voltage drop across impedance matching diode 44. The added voltage drop across impedance matching diode 44 serves to maintain the voltage current relationship between tunnel diode 33 and the emitter-base of transistor 11 as illustrated in FIGURE 2 of the drawings.

FIGURE 4 is a detailed circuit diagram of a practical high frequency chopper circuit constructed in accordance with the present invention. In the circuit of FIGURE 4, a PNP power transistor 11 has its emitter-collector connected through the primary winding 15 of a saturable core transformer 16 and a load 17 across the terminals (+ and -) of a direct current power supply. The primary winding 15 is wound on a common core member with a secondary winding 18, a reset winding 27, a first control winding 51, and a second control or turn off winding 52 all of which are of course inductively coupled to the primary winding 15 through the medium of the common saturable core member. The reset winding 27 is connected in series circuit relationship with a pair of resistors 24 and 25 across the emitter-collector of power transistor 11, and hence are connected across the terminals (+ and -) of the direct current power supply through primary winding 15 and load 17. The dot end of the secondary winding 18 is connected to the junction of the bias resistors 24 and 25, and the no dot end of winding 18 is connected through an impedance matching diode 44 to the base of the power transistor 11. The no dot end of secondary winding 18 is also connected through a pair of series connected bias resistors 53 and 54 to the positive terminal of the direct current power supply with the junction of the bias resistors 53 and 54 being connected directly to the base of power transistor 11. The series cir-

cuit comprised by the impedance matching diode 44 and the emitter-base of power transistor 11 is connected in parallel circuit relationship with a series circuit comprised by a tunnel diode 33 and series connected blocking diode 41. A clamping diode 55 shown in solid line is operatively connected in parallel circuit relationship across the emitter-base of power transistor 11 in a reverse polarity sense with respect to the blocking diode 41. The purpose of the clamping diode 55 will be appreciated more fully hereinafter. If desired, the clamping diode 55 may be connected in the manner shown by the dotted diodes 55 to accomplish the same purpose.

Continuous control over the load current supplied to the load 17 by the circuit arrangement of FIGURE 4 is accomplished with the first control winding 51 which is connected in series circuit relationship with a diode 56 across the emitter-collector of an NPN junction transistor 57. The NPN junction transistor 57 has its emitter-base connected to a source of continuously variable control signals which of course will vary the conductance of the NPN junction transistor 57. Similarly, the second control turn off winding 52 is connected in series with a diode 58 across the emitter-collector of an NPN junction transistor 59 with its base connected to a source of turn off control signals.

Consider the power transistor 11 to be in its non-conducting condition and that the core of the saturable core transformer 16 has been driven into its negative saturation condition by the reset current flowing in the reset winding 27 at the end of a previous cycle of operation. With the circuit in this condition, a small negative bias will be applied from the bias resistors 24 and 25 to the cathode of tunnel diode 33 and to the base of PNP power transistor 11. This causes the tunnel diode to be rendered conductive and causes a small emitter-base current to flow in the power transistor 11 as explained in connection with FIGURES 1 and 2. This small emitter-base current is sufficient to cause a collector current to flow through the primary winding 15 that will cause the core of transformer 16 to be unsaturated, and to induce a potential in the secondary winding 18 which is negative at the no-dot end. This induced potential in the secondary winding 18 is regenerative and causes a larger current flow through the tunnel diode 33, and a larger emitter-base current flow through a power transistor 11. Thereafter, as the current flow through the tunnel diode 33 increases to the point a in FIGURE 2 so that it is switched to its high voltage mode of operation, the power transistor 11 will be switched to its full on condition almost instantaneously. This increases the collector current flow, hence the load

current flow, and continues driving the core of saturable core transformer 16 towards its positive or opposite condition of saturation. Thereafter, the power transistor 11 will continue to conduct and supply load current through the load 17 for the period of time required to drive the core of saturable core transformer 16 into positive saturation.

Upon the core of saturable core transformer 16 reaching positive saturation, the primary and secondary windings 15 and 18 will be decoupled so that the potential across winding 18 drops essentially to zero. With the potential across the winding 18 substantially zero, the bias potential continuously applied from the bias resistors 53 and 54 to the base of power transistor 11 will take over and reverse bias the base-emitter of the power transistor 11 thereby causing it to turn off almost instantaneously. This instantaneous application of the reverse bias across the emitter-base of power transistor 11 is made possible by the presence of the blocking diode 41 which prevents the reverse bias from being dissipated through tunnel diode 33. The application of reverse bias also returns the tunnel diode to its low voltage state.

At the instant that the power transistor 11 is turned off, the load current through the primary winding 15 will decay to zero almost instantaneously, and the collapsing lines of flux in the saturable core transformer 16 will unsaturate the core of transformer 16 and generate in the secondary winding 18 a reverse polarity potential which now will be positive at the no dot end of winding 18. In order to dissipate this induced potential across winding 18 during turn off, the clamping diode 55 is provided thereby avoiding any risk of injury to the emitter-base of the power transistor 11. It should be noted that the clamping diode may be connected in the manner shown in solid lines, or alternatively may be connected as shown by the dotted outline form, or in any other manner so long as it effectively shunts the emitter-base of the power transistor 11 insofar as this reverse polarity potential generated by winding 18 is concerned.

With the power transistor 11 turned off in the above described manner, the circuit is returned to its initial condition of operation ready for a new cycle of operation. By varying the value of the continuously variable control signal E_{con} applied to the base of the transistor 57, the point at which the core of saturable core transformer 16 reaches positive saturation to thereby initiate turn off of the power transistor 11 in the above described manner, can be varied to thereby vary the period of conduction or time on of the power transistor 11. The circuit described enables variation of the value of the load current being supplied to load 17 in a

proportional control manner as described in U.S. Patent No. 3,102,206. In the event of the application of the turn-off signal E_{to} to the base of the transistor 59, the circuit of FIGURE 4 will be turned off practically concurrently with application of the turn-off signal thereby making it possible to protect the power transistor in the circuit from possible damage. It should also be appreciated that the number of additional turn-off windings such as 52 which can be added to the saturable core transformer 16 is practically limitless (within reason) since these windings do not effect operation of the circuit until a turn-off signal is applied to them. For this reason, the circuit makes it possible to provide multiple insulated input signals to the circuit which are effectively isolated from the power current flowing in the power circuit.

FIGURE 5 of the drawings is an equivalent circuit arrangement of the circuit shown in FIGURE 4. With respect to FIGURE 5, the switches 32 and 43 are effectively provided by the winding 18 of saturable core transformer 16 which, dependent upon its condition whether saturated or unsaturated, the switch is either open or closed. With winding 18 in its saturated condition, the circuit operates as though switch 43 were closed in FIGURE 5 and switch 32 opened. With winding 18 in its unsaturated condition, the circuit operates as though the switch 32 were closed and the switch 43 were opened.

FIGURE 6 of the drawings illustrates the basic circuit configuration of a form of high frequency chopper circuit having a constant frequency output and wherein the time on of the power transistor is varied to thereby vary the load current supplied to a load through the power transistor. In the circuit arrangement of FIGURE 6 a power transistor 11 has its emitter-base coupled across the secondary winding 18 of a saturable core transformer 16. The secondary winding 18 is wound in common on a toroidal core member 61 with a primary winding 15 and a control winding 51 in a conventional fashion. Primary winding 15 is here connected to a separate source of square wave alternating current potential having the wave form illustrated at 62 through a current limiting resistor 63. The control winding 51 is connected through a diode 56 across the emitter-collector of an NPN junction transistor 57 whose base is connected to a source of control signals E_{con} .

For the purpose of illustration, first consider the case where there is no control signal E_{con} applied to transistor 57, and hence control winding 51 has no effect on the operation of the circuit. Consider also that the core of saturable core transformer 16 has been driven into negative saturation by the previous negative half cycle of the square

wave alternating current potential 62 supplied to primary winding 15. Under these circumstances, the positive half-cycle of the square wave alternating current potential 62 will drive the core of saturable core transformer 16 out of negative saturation and tend to reset it towards positive saturation. As a consequence, a potential will be developed in the secondary winding 18 which is positive at the dot end and which will cause power transistor 11 to be turned on. The power transistor 11 will then be maintained turned on for the period of time required for the core of saturable core transformer 16 to be driven into positive saturation by the positive half-cycle of the square wave alternating current potential 62. By proper design of the core of transformer 16 and the windings 15, 51, and 18, the transformer 16 can be designed so that its core is driven into positive saturation at the termination of the positive half-cycle of the square wave alternating current potential 62 assuming no control signal is applied to the transistor 57. Upon reaching positive saturation, the potential across winding 18 will drop to zero. As a consequence, the emitter-base current of transistor 11 decreases to zero and the power transistor 11 will start to turn off. During the succeeding negative half-cycle of the square wave alternating current potential 62, the core of saturable core transformer 16 will be driven out of positive saturation towards negative saturation and will develop a reverse polarity potential across the winding 18 which is now positive at the no-dot end. As a consequence, the power transistor 11 will be turned full off during the negative half-cycle of square wave potential 62, and the core of the saturable core transformer 16 will be driven back into negative saturation during the negative half-cycles.

Consider now the effect of the transistor 57 and diode 56. By reason of the polarity of the connection of the diode 56, the diode will block any current flow during the positive half-cycles of the square wave potential 62 so that no current can flow through winding 51 during the positive half-cycles, and hence the winding will have no effect during these periods. However, during the negative half-cycles of the applied square wave potential 62 an enabling potential e_r of the proper polarity will be developed across the winding of transistor 57. If under these conditions the control signal E_{con} which is positive in nature is applied to the base of the transistor 57 the transistor will be turned on. The amount of current that is allowed to flow 51 which is applied across the collector-emitter through the transistor will of course be determined by the value of the control signal E_{con} . From a consideration of FIGURE 6 it can be appreciated that the ampere turns caused by the winding 51 oppose the ampere turns

of primary winding 15 during the negative half-cycle of the square wave alternating current potential 62. Therefore in effect the control winding 51 controls the degree of reset of the core of saturable core transformer 16 during the negative half-cycles of potential 62. By thus controlling the degree of reset, or the extent to which the core of saturable core transformer 16 is driven toward negative saturation during the negative half-cycles of the applied square wave alternating current potential 62, the control winding 51 in effect sets the amount of time which will be required for the succeeding positive half-cycle of the square wave alternating current potential 62 to drive the core 61 into positive saturation, and hence, thereby controls the on time of the power transistor 11. Thus, it can be appreciated that the power transistor 11 will be turned on at a constant frequency rate, but that its on time is varied to thereby vary the value of the load current being supplied through the power transistor.

FIGURE 7 of the drawings illustrates the manner of operation of the circuit of FIGURE 6. FIGURE 7 (a) illustrates the voltage-time characteristic of the square wave alternating current potential 62 applied to primary winding. In FIGURE 7 (b), the current versus time characteristic of the base current i_b is shown for the condition where the core of saturable core transformer 16 is driven into positive saturation at about 120° phase relation with respect to the applied square wave switching potential 62. The potential e_r appearing across the control winding 51 is illustrated in FIGURE 7 (c). By varying the value of the control signal E_{con} supplied to the base of transistor 57 the value of i_b can be either increased or decreased to thereby vary the on time (and hence load current) of the power transistor 11 in a desired fashion.

FIGURE 8 of the drawings illustrates a practical circuit configuration for a constant frequency, high speed, time-ratio control, power chopping circuit constructed in accordance with the principles of the present invention. The circuit arrangement of FIGURE 8 is identical to the circuit of FIGURE 6 with the exception that a tunnel diode 33 and blocking diode 41 are connected in series circuit relationship across the base-emitter of power transistor 11 and a series connected impedance matching diode 44. By the addition of these elements to the circuit arrangement of FIGURE 6, high speed turn on of the power transistor 11 can be accomplished in the manner described more fully with relation to FIGURES 1 and 2 of the drawings.

In order to accomplish high speed turn off of the power transistor 11 in FIGURE 8, a source of reverse polarity potential is con-

connected in parallel circuit relationship with the emitter-base of power transistor 11. This source of reverse polarity potential may be a battery or other suitable d.c. source, but in the specific arrangement shown in FIGURE 8, is comprised by a rectifier circuit 64 and series connected resistor 65 connected across the emitter-base of power transistor 11. The rectifier circuit 64 is comprised by a pair of diodes 66 and 67 connected in back-to-back relationship across the secondary winding 68 of a coupling transformer whose primary winding 69 is coupled to the source of square wave alternating current potential 62 applied to primary winding 15 of saturable core transformer 16. By this arrangement, upon the secondary winding 18 being driven into positive saturation, the reverse polarity potential developed across the resistor 65 will reversely bias emitter-base of power transistor 11 to cause it to quickly turn off. A clamping diode 55 operatively connected in parallel with the emitter-base of power transistor 11 will serve to clamp the emitter-base potential to the voltage drop across the diode and tunnel diode 33 during turn off thereby avoiding any possible damage to the power transistor 11.

FIGURE 9 of the drawings shows a form of high frequency chopping circuit which can be applied to the simplified bridge inverter network of FIGURE 10 to provide either an alternating current output voltage or a reversible polarity direct current output voltage depending upon how the network is operated. FIGURE 9 shows the respective switching transistors 11a and 11b in the two arms of the bridge forming one of the two parallel branches between the input terminals marked + and - in FIGURE 10. For the purpose of the present discussion, ignore for the time being the lower half of the circuit including the power transistor 11b and its associated circuitry and the two pulse transformers 71 and 72. The saturable core transformer 16 in the circuit arrangement shown in FIGURE 9 is in fact two saturable core transformers 16 and 16' which in effect operate similarly to the transformer 16 previously described. However, in the circuit arrangement of FIGURE 9, one of the saturable core transformers 16 operates on one-half cycle of the applied square wave alternating current potential 62 as discussed in connection with the circuit of FIGURE 6, and the remaining saturable core transformer 16' operates on the opposite half-cycle so that the two together provide full wave control to the power transistor 11a similar to a full wave magnetic amplifier. With the control signal E_{con} applied to the transistor 57 equal to zero, the power transistor 11a will be turned on or conducting for a full 360° of the square wave alternating current potential 62. As the value of the control signal E_{con}

is increased, the conducting time of the power transistor 11a is reduced proportionally until it finally reaches zero for E_{con} equal to full value. Full wave operation of the power transistor 11a in this manner provides a chopping rate which is double the frequency of the square wave alternating current potential 62.

With the circuit thus far described, therefore, it can be appreciated that the control voltage E_{con} controls the output voltage to the load. Since the control windings 51, 51' of the saturable core transformers 16 and 16' are wound on separate parts of the core from the primary and secondary windings, the separation of the windings isolates the input circuits from each other and from the power output circuit, and in addition provides insulation. Pulses of voltage, fast rise time in voltage, etc. between the various input control circuits and the output power circuit do not disturb the input controls applied to the circuit. Further, as explained in connection with FIGURE 4, additional multiple input and turn off controls can be applied to the core members of the saturable core transformers 16, 16' to provide any desired number of inputs which are insulated and isolated from each other and from the power load circuit as well.

Considering now the effect of the lower half of the circuit shown in FIGURE 9 including the power transistor 11b where such a control circuit is included as the left half control for a bridge circuit such as that illustrated in FIGURE 10, for example. A bridge circuit so constructed can be employed to develop either an alternating current potential or a reversible polarity variable direct current output voltage across the load depending upon the nature of the control signals supplied to circuit. It is to be understood that a right hand control circuit similar to that of FIGURE 9 would be connected to the power transistors 11a' and 11b' of the circuit shown in FIGURE 10 for such operation, however.

The control circuit for the power transistor 11b is slaved to the control circuit of power transistor 11a in the circuit arrangement shown in FIGURE 9. The pulse transformers 71 and 72 supply pulses to the control gates of a pair of silicon controlled switches (SCS) 73 and 74 that are connected through a limiter resistor 75 and impedance matching diode 44b to the base of power transistor 11b. Alternating current power is supplied to the silicon controlled switches 73 and 74 through a supply transformer 76 having its primary winding coupled to the source of square wave alternating current potential 62. The tunnel diode switching circuit comprised by tunnel diode 33b and working diode 41b assures fast turn on of the power transistor 11b, and fast turn off of power transistor 11b

is accomplished through the rectifiers 64b and resistor 65b which reverse bias the emitter-base of power transistor 11b.

By the above arrangement, power transistor 11b is turned on at the time that power transistor 11a is turned off. The tunnel diode fast switching circuit including tunnel diode 33b switches the power transistor 11b in a fast manner the same as diode 33 in the circuit arrangement of FIGURE 8. When the core of the saturable core transformers 16 or 16' saturates, the flux in the cores of the pulse transformers 71 or 72 drops to the residual flux level, and a voltage is induced in the secondary windings of the pulse transformers 71 or 72 to thereby turn on the SCS 73 or SCS 74. Turn on of SCS 73 or SCS 74 results in fast turn on of power transistor 11b. When incorporated in a bridge arrangement such as shown in FIGURE 10, the right hand power transistors 11a' and 11b' forming the two arms of the second branch of the inverter, are controlled by an identical circuit to the one controlling power transistors 11a and 11b so that the control circuits can be used in series. With such an arrangement the emitter of the control transistor 57 used for the left side of the bridge would be connected to the emitter of the corresponding control transistor 57 used on the right side of the bridge circuit, and the control signal input is applied to the bases of both transistors.

By reason of the above construction, a transistor-magnetic power amplifier is made available having multiple insulated and isolated inputs. The high speed chopping amplifier employs a technique of time ratio control and provides lightweight, compactness, high efficiency and high reliability operation at very high switching speed made possible by the use of high speed power transistors used in conjunction with tunnel diode high speed switching circuits to permit high chopping frequencies. The multiple inputs made possible by the circuit permit take over control for such purposes as current limit, thermal limits, under voltage or over voltage, etc., and the isolation of the multiple inputs from each other and from the power output permit the take over controls to operate in circuits having high dv/dt which otherwise might interact on each other to cause circuit failure.

From the foregoing description, therefore, it can be appreciated that the invention makes available high speed chopping circuit arrangements which employ a high speed power transistor and a tunnel diode to accomplish high speed switching of the base current of the transistor to thereby achieve high chopping frequencies. The circuits thus comprised also employ saturable core transformers and these may be provided with multiple insulated inputs that are effectively

isolated from each other and from the high frequency power derived at the output of the circuit.

WHAT WE CLAIM IS:—

1. A switching circuit comprising a transistor; a tunnel diode connected between the emitter and base of the transistor with like polarity to the emitter-base junction; and a saturable transformer having a first winding and a second winding which is coupled to the base and emitter of the transistor to apply switching signals thereto.

2. A switching circuit according to Claim 1, wherein said first winding is connected in the base collector circuit of the transistor to form a regenerative circuit for turning on said transistor.

3. A switching circuit according to Claim 1, coupled to said first winding to control the switching of said transistor.

4. A switching circuit according to any preceding claim comprising a rectifier diode connected between the emitter and base of the transistor in series circuit relationship with the tunnel diode to conduct current in the same direction as the tunnel diode.

5. A switching circuit according to Claim 4 comprising an impedance-matching diode connected in series circuit relationship with the emitter-base junction of the power transistor to conduct current in the same direction as the junction, the tunnel diode being connected in parallel circuit relationship with the series circuit comprising the emitter-base junction of the power transistor and the impedance-matching diode.

6. A switching circuit according to any preceding claims, comprising a clamping diode in parallel circuit relationship with the emitter-base junction of the power transistor and connected in a reverse polarity sense with respect to the tunnel diode.

7. A switching circuit according to any preceding claim, wherein said saturable transformer has a further winding for receiving current to control the saturating of the transformer core, and further comprising means for applying current to said control winding to thereby control the switching of said transistor.

8. A switching circuit according to any one of Claims 1 to 6, wherein said saturable transformer has two further windings for receiving currents to control the saturating of the transformer core, and further comprising means for applying currents to said further windings such that the current in each winding controls the switching off of the transistor.

9. A switching circuit according to Claim 7 or 8 when dependent on Claim 2, wherein said saturable transformer has a reset winding coupled in the base-collector circuit of said transistor to provide current for saturat-

ing the core of the transformer in one polarity prior to switching on of the transistor.

- 10 10. A switching circuit according to Claim 6 comprising means for providing turn-off
5 current to the transistor, and connected in parallel circuit relationship with the emitter-base junction of the power transistor and the second winding of the saturable transformer.

- 10 11. A bridge inverter circuit comprising a transistor in each arm of the bridge to switch current in that arm, a respective tunnel diode connected between the emitter and base of each transistor and with like polarity
15 to the emitter-base junction, and one of the transistors in each branch of the bridge between the input terminals thereof having

associated therewith a respective saturable transformer with a first winding for receiving current to effect saturation of the transformer 20 and a second winding coupled to the base and emitter of the associated transistor to apply switching signals thereto.

12. A switching circuit substantially as hereinbefore described with reference to Fig- 25 ure 4; Figure 8 or Figures 9 and 10 of the accompanying drawings.

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FIG. 1 (a)

(b)

(c)

FIG. 2

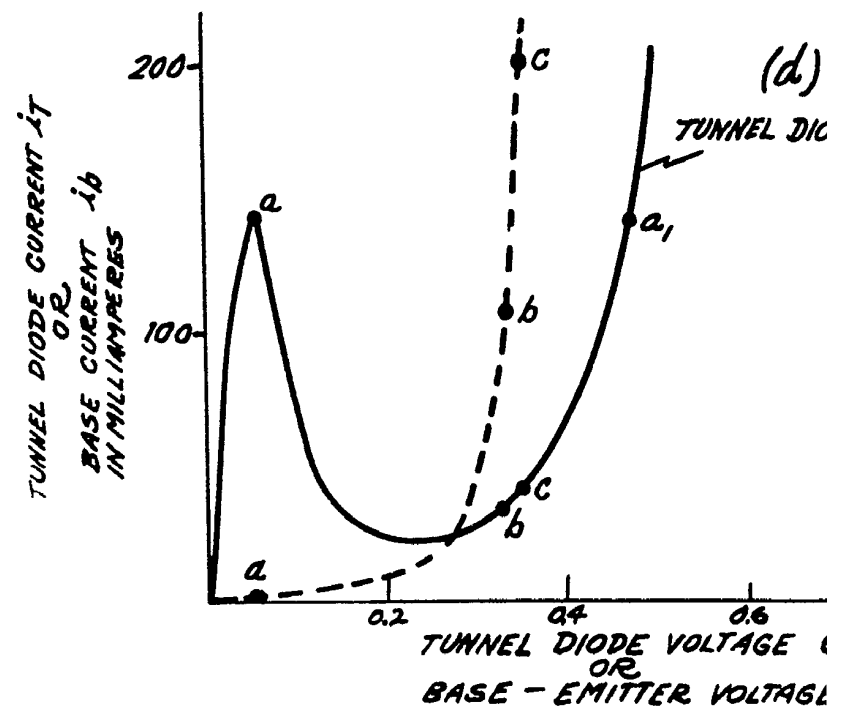
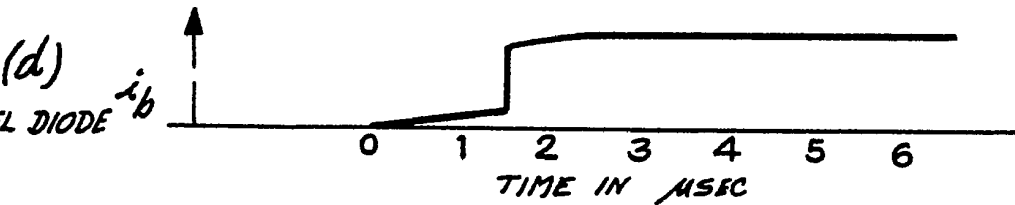
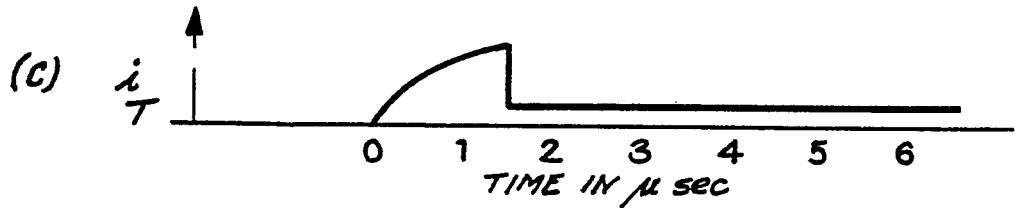
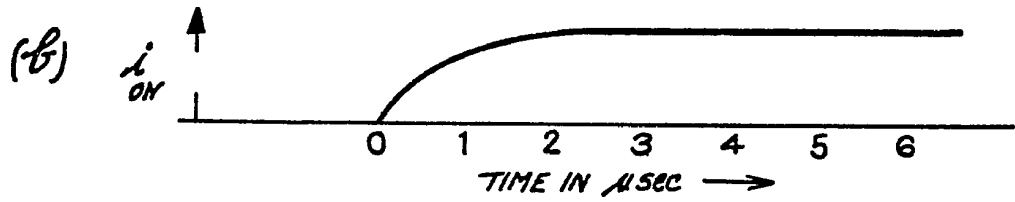
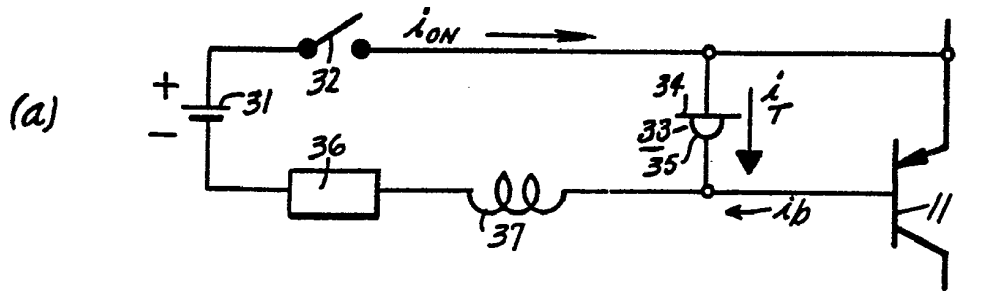
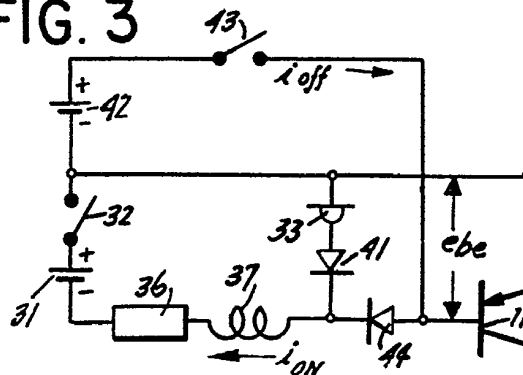


FIG. 1



TUNNEL DIODE
 a_1

FIG. 3



0.6 0.8
 BDE VOLTAGE e_T
 OR
 TITTER VOLTAGE e_{be} IN VOLTS

FIG. 1

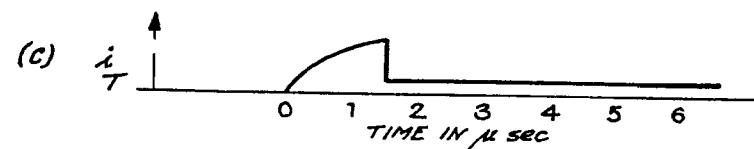
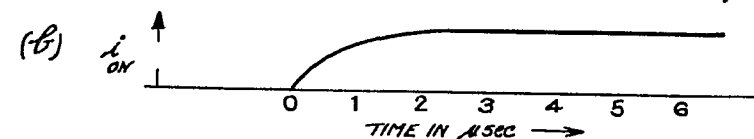
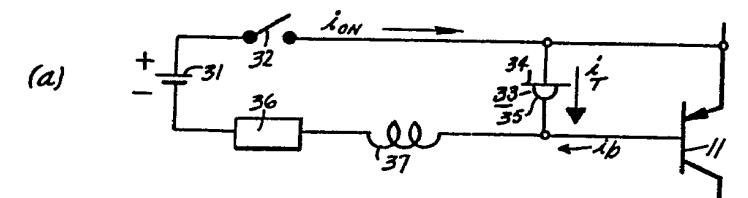


FIG. 2

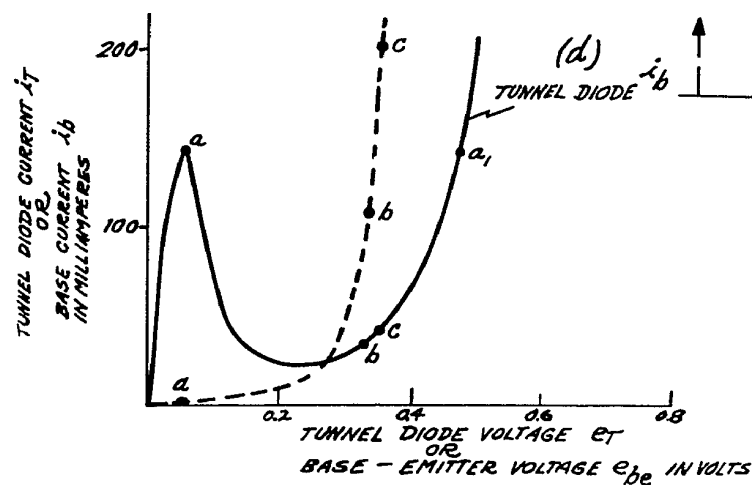


FIG. 3

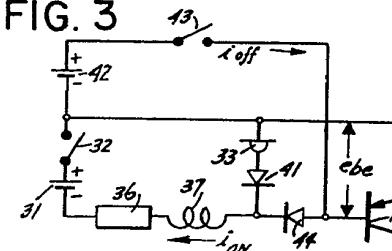


FIG. 4

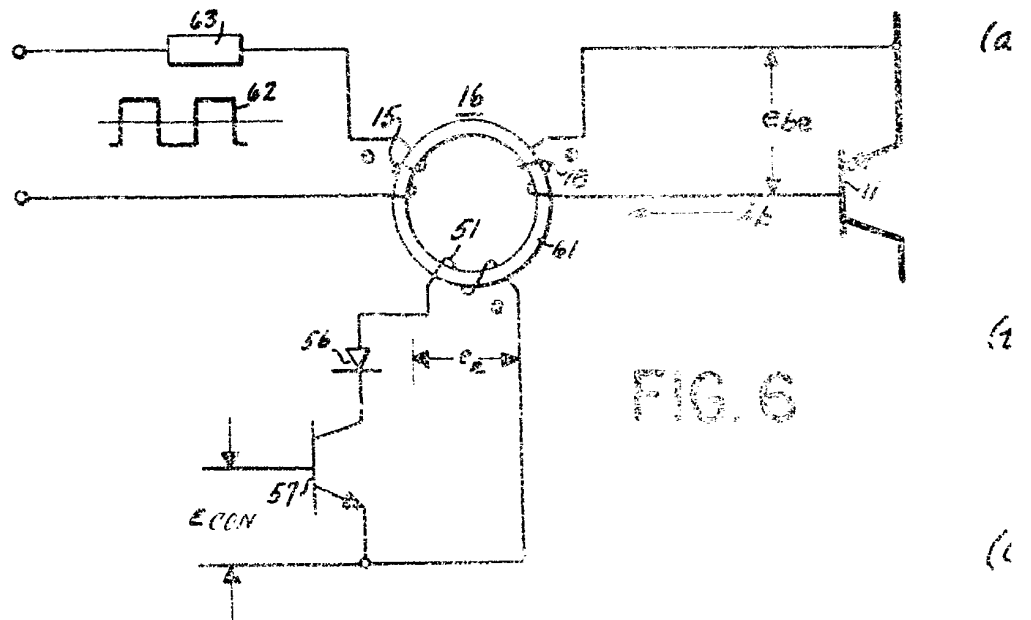
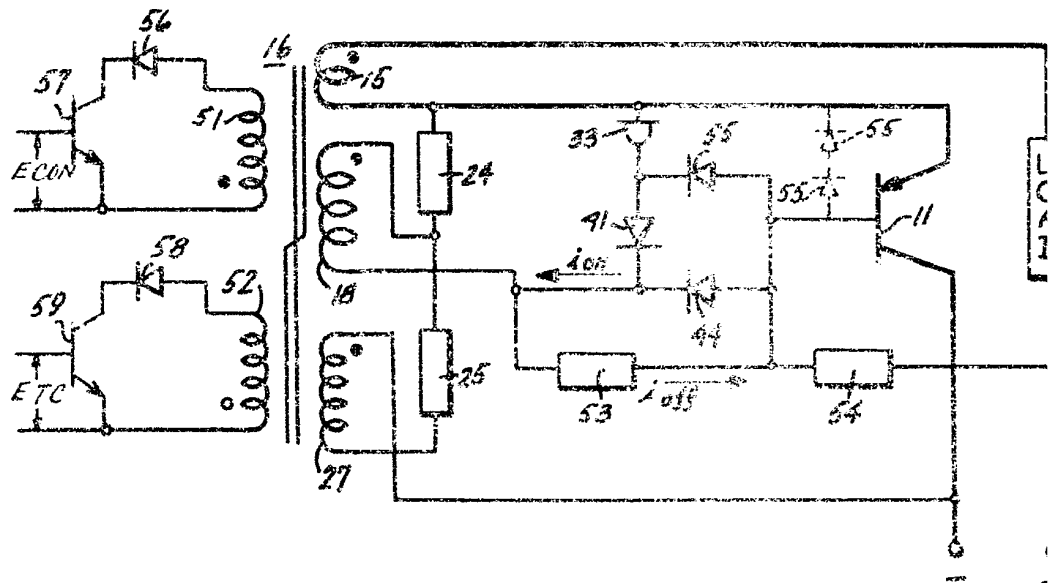


FIG. 6

FIG. 5

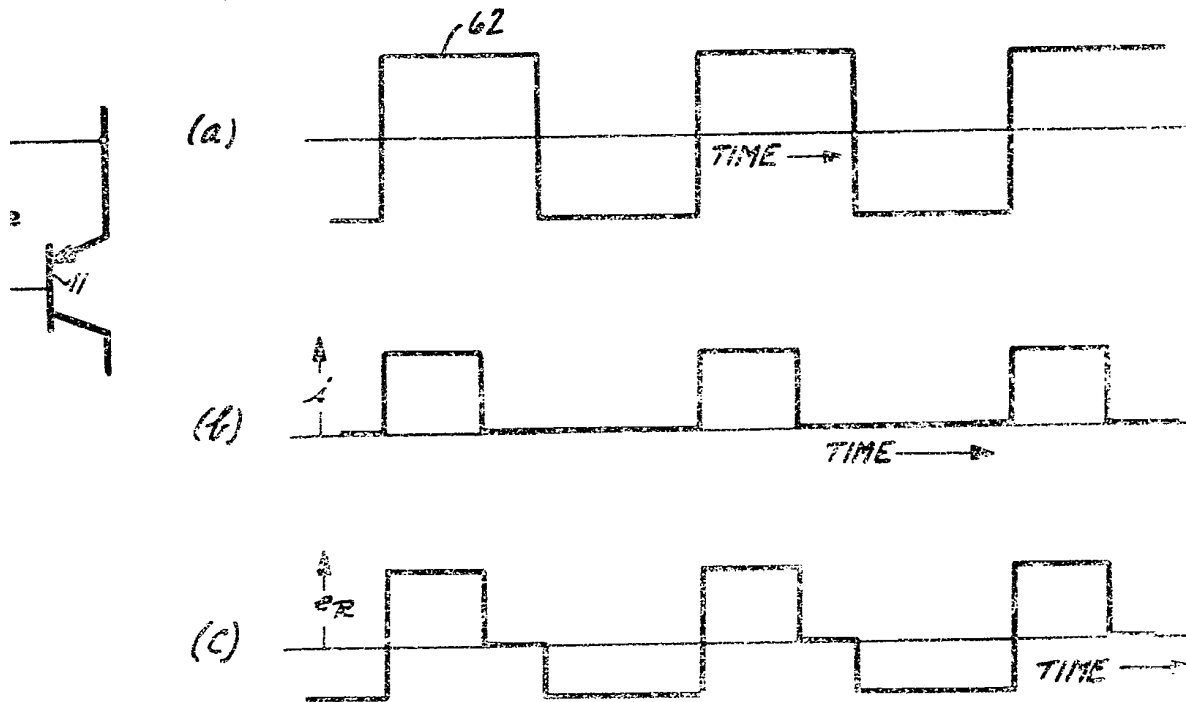
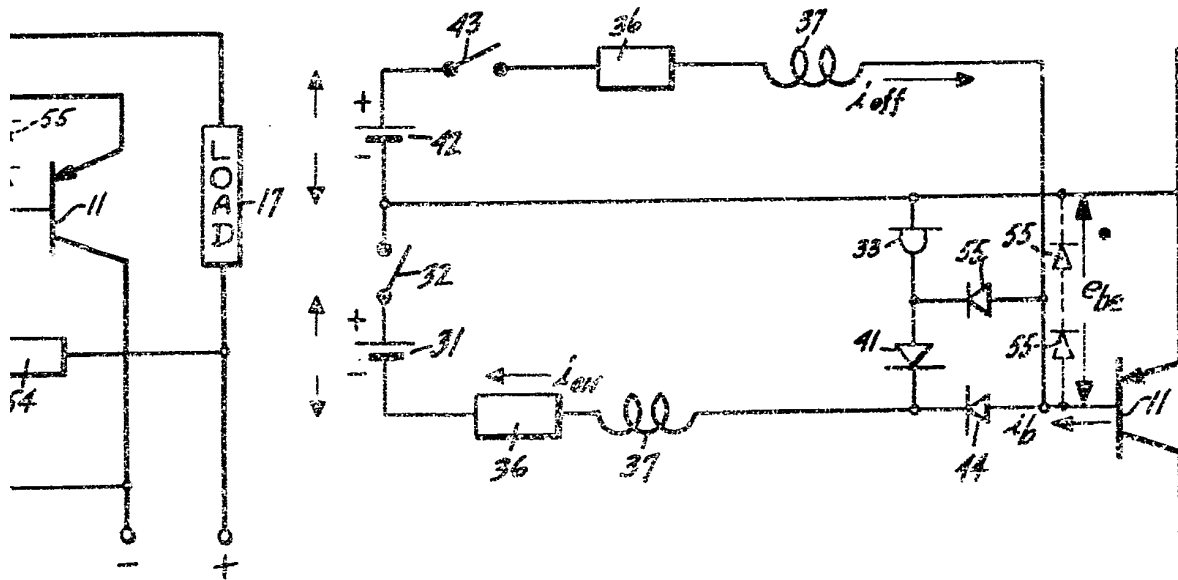


FIG. 7

FIG. 4

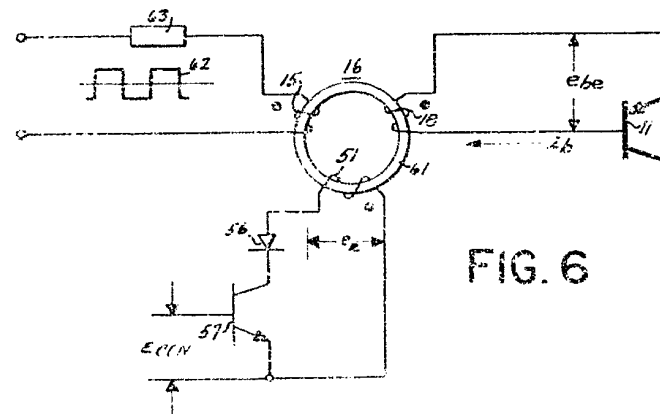
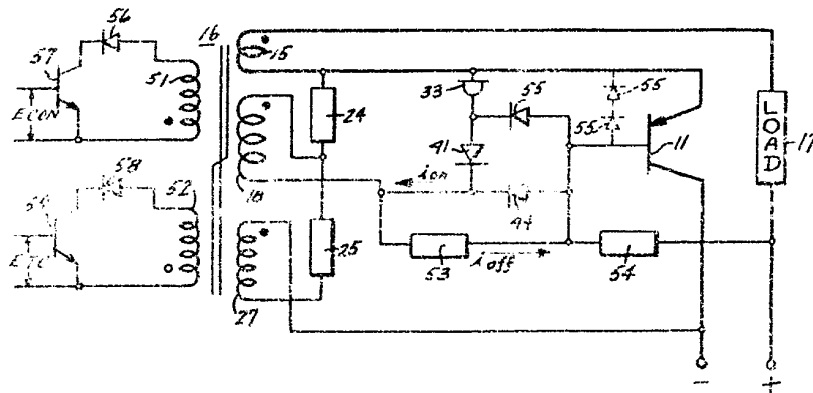


FIG. 6

FIG. 5

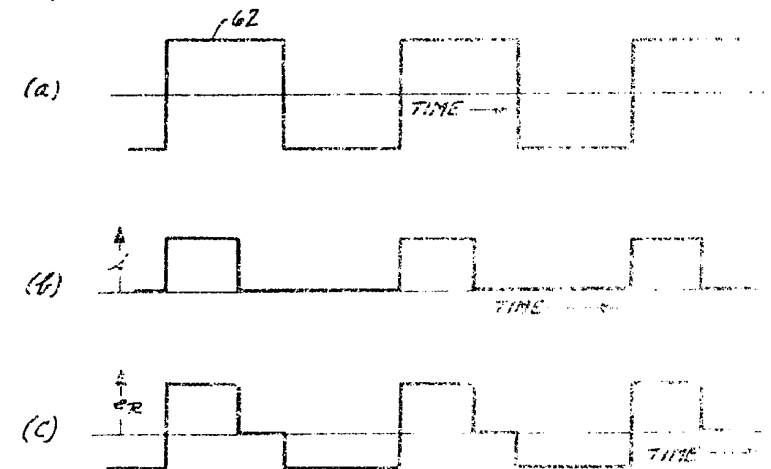
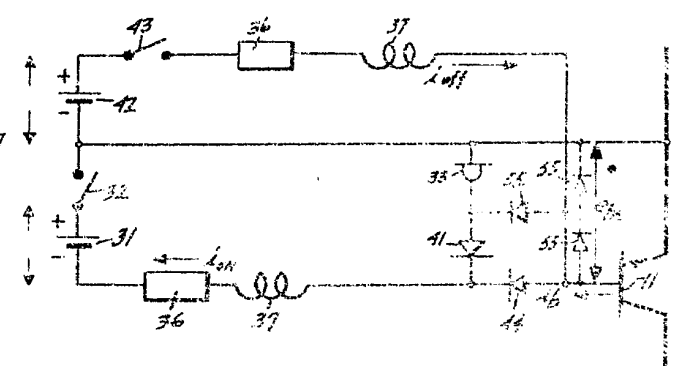


FIG. 7

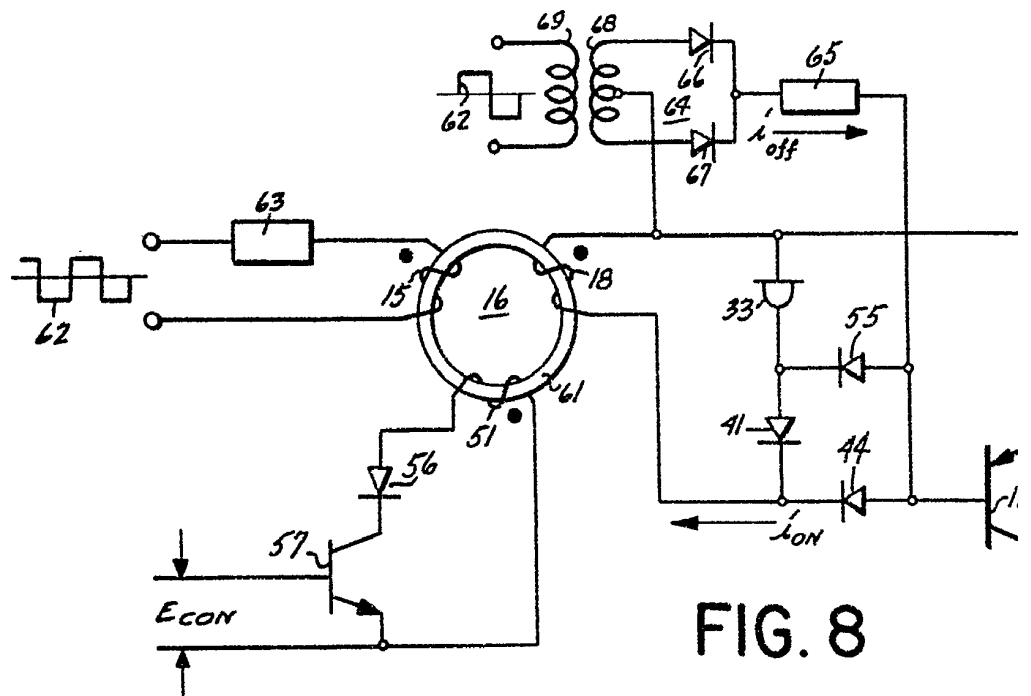


FIG. 8

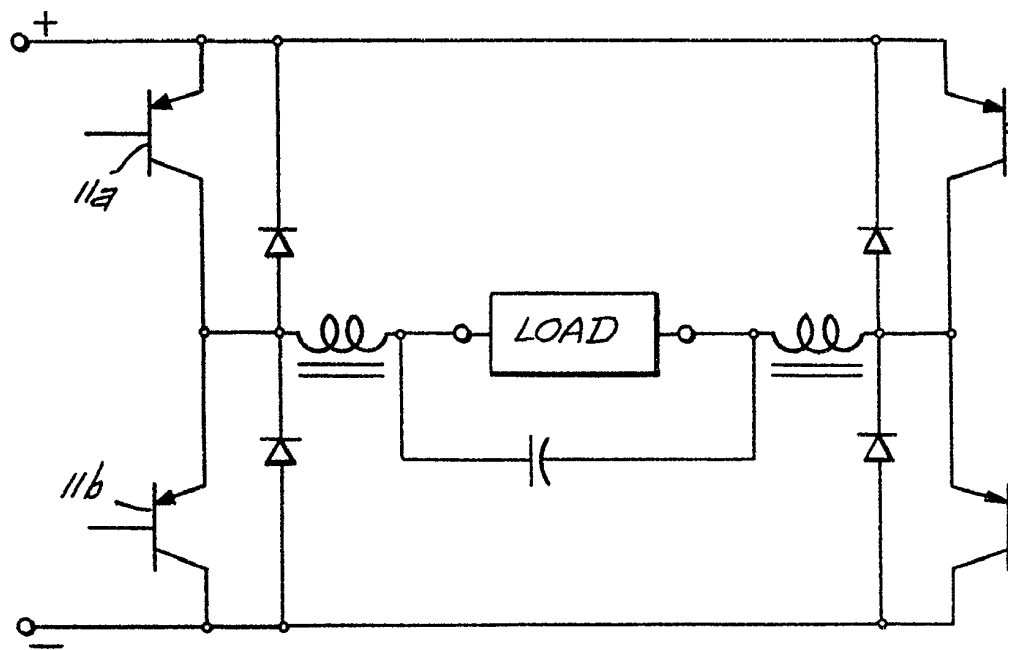


FIG. 10

FIG. 9

