



Express Search

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Mr. Express Search Internal
Express Search, Inc
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Re:
Patent Validity Search
Quantum-Well Logic Using Self-Generated Potentials
Express Search Sample Validity Search

June 18, 2019

Dear Mr. Search,

In accordance with your e-mail received on June 11, 2019, a Patent Validity Search was conducted using priority date of July 2, 1984 and 1, 6, 7, 8, 13, 14 for U.S. Patent 4,969,018.

A new kind of electronic logic circuit, wherein potential wells (e.g. islands of GaAs in an AlGaAs lattice) are made small enough that the energy levels of carriers within the wells are discretely quantized. This means that, when the bias between the wells is adjusted to align energy levels of the two wells, tunneling will occur very rapidly, whereas when the energy levels are not aligned, tunneling will be greatly reduced. In particular, the wells are optimized to have sharp enough resonant tunneling peaks that the change in potential caused by the difference between the number of carriers stored between two adjacent tunnel wells is itself enough to permit or preclude resonant tunneling. Thus, a tremendous variety of logic functions, including all primitive Boolean functions can be embodied in this logic.

Claims

Claim 1. A semiconductor logic device, comprising:

(a) a plurality of quantum wells, said wells separated by tunneling barriers and of size to quantize all three components of momentum of carrier in said wells;

(b) at least one pair of adjacent ones of said wells having carrier states that are in resonance only if the carrier population of a first of said pair differs from the carrier population of the other of said pair; and

(c) at least one input and output for said plurality, whereby carriers injected by said input into certain of said wells resonantly tunnel unidirectionally from well to well and are withdrawn from certain of said wells by said output.

Claim 6. The semiconductor logic device of claim 1, wherein:

(a) said plurality includes first, second, third, and fourth wells with resonant carrier states as follows: (i) one carrier in said first well with no carriers in said third well, (ii) one carrier in said second well with one carrier in said third well, and (iii) two carriers in said third well with no carriers in said fourth well, whereby after resonant tunneling said fourth well occupation is a logical AND of said first and second well occupations.

Claim 7. The semiconductor logic device of claim 1, wherein:

(a) said plurality includes first, second, third, and fourth wells with resonant carrier states as follows: (i) one carrier in said first well with no carriers in said third well, (ii) one carrier in said second well with no carriers in said third well, and

(iii) one carrier in said third well with no carriers in said fourth well, whereby after resonant tunneling said fourth well occupation is a logical OR of said first and second well occupations.

Claim 8. A semiconductor logic device, comprising:

(a) a plurality of quantum wells, said wells separated by tunneling barriers and of size to quantize all three components of momentum of carriers in said wells;

(b) at least two of said wells of unequal single carrier energy states such that the presence of carriers in a first of said two wells is necessary for resonance of carrier states between said two wells; and

(c) at least one input and output for said plurality, whereby carriers injected by said input into certain of said wells resonantly tunnel unidirectionally from well to well and are withdrawn from certain of said wells by said output.

Claim 13. The semiconductor logic device of claim 8, wherein:

(a) said plurality includes first, second, third, and fourth wells with resonant carrier states as follows: (i) one carrier in said first well with no carriers in said third well, (ii) one carrier in said second well with one carrier in said third well, and (iii) two carriers in said third well with no carriers in said fourth well, whereby after resonant tunneling said fourth well occupation is a logical AND of said first and second well occupations.

Claim 14. The semiconductor logic device of claim 8, wherein:

(a) said plurality includes first, second, third, and fourth wells with resonant carrier states as follows: (i) one carrier in said first well with no carriers in said third well, (ii) one carrier in said second well with no carriers in said third well, and (iii) one carrier in said third well with no carriers in said fourth well, whereby after resonant tunneling said fourth well occupation is a logical OR of said first and second well occupations.

The search was conducted in accordance with the disclosure provided.

The following references for 'Quantum-Well Logic Using Self-Generated Potentials' appear to be most relevant:

4,575,924 [Reed et al] discloses quantum well device made by etching trenches to two levels through epitaxial layers and refilling with lattice matched wider band gap semiconductor for paired quantum wells (Claims 1-3).

4,503,447 [Iafrate et al] discloses multi-dimensional quantum well device with high-mobility, low band-gap regions in low-mobility high band-gap layer (Column 3, Lines 50-66; Column 4, Lines 30-59).

4,912,531 [Reed et al] discloses 3-terminal quantum device with multiple potential wells containing lightly doped semiconductors (Claims 1g, 13a, 13g, 25a, and 25g).

4,581,621 [Reed] discloses a multiple quantum well device with output switch and trapping site close to one well closely coupled to fine metal wire (Claim 1).

5,032,877 [Bate] discloses quantum-coupled ROM with information encoded in pattern of coupling column lines to changes of wells linked by resonant tunneling (Claims 1-6).

4,439,782 [Holonyak] discloses heterojunction semiconductor device with a binary semiconductor active layer and different binary semiconductor barrier layers.

JPS 5990978A [Yanase et al] discloses superlattice-structure negative-resistance element has two mixed-crystal semiconductor thin-films with different energy bands formed alternately.

4,620,206 [Ohta et al] discloses semiconductor device with negative resistance from pairs of superlattice semiconductor thin films which are laminated such that films are monotonically changed in lamination direction.

JPS 5967676A [Yanase et al] discloses negative resistance element obtaining large amplification from 2 kinds of mixed crystal semiconductor thin film layers formed in lamination.

The following non-patent literature articles were uncovered during the search:

Barker, J. R., and D. K. Ferry. "On the physics and modeling of small semiconductor devices-II: The very small device." Solid-State Electronics 23.6 (1980): 531-544.

<http://www.sciencedirect.com/science/article/pii/0038110180900349>

Disclosing normal PMMA as used extensively in electronbeam lithographic processing of LSI circuits, can be utilized to differentiate value in the same order as that expected from Josephson junction logic with layers completely depleted with the electrons falling into the GaAs potential wells. Published as three texts.

Sollner, T. C. L. G., et al. "Resonant tunneling through quantum wells at frequencies up to 2.5 THz." Applied Physics Letters 43.6 (1983): 588-590.

<http://scitation.aip.org/content/aip/journal/apl/43/6/10.1063/1.94434>

Disclosing well influencing low-density transit time estimate by about a factor of 2. The tunneling current density of these devices is rather low for practical applications in view of the large capacitance.

Chang, L. L., Leo Esaki, and R. Tsu. "Resonant tunneling in semiconductor double barriers." Applied Physics Letters 24.12 (1974): 593-595.

http://nashaucheba.ru/docs/6/5419/conv_26/file26.pdf

Disclosing resonant tunneling of electrons in double-barrier structures (fabricated by molecular beam epitaxy which produces extremely smooth films and interfaces) with a thin GaAs sandwiched between two GaAlAs barriers as peaks/humps in the tunneling current at voltages near the quasi-stationary states of the potential well.

Wilamowski, Bodgan M. "Schottky diodes with high breakdown voltages." Solid-State Electronics 26.5 (1983): 491-493.

http://www.eng.auburn.edu/~wilambm/pap/1983/SSElektr_SchottkyDiodes.pdf

Discloses increasing the breakdown voltages in silicon Schottky diodes with screen-diffusion regions introduced to a guarding ring to lower the electrical field near the Schottky contact resulting in higher breakdown voltages increased by a factor of 3-5. However, a large device area is required for the same Schottky contact area and, therefore, the junction parasitic capacitance is greater.

Frey, Jeffrey. "Simulation of Submicron Si and GaAs Devices: Problems and Techniques." Simulation of Semiconductor Devices and Processes: Proceedings of an International Conference Held at University College of Swansea, Swansea, UK on July 9th-12th, 1984. Vol. 1. Pine Ridge Press, 1984.

http://in4.iue.tuwien.ac.at/pdfs/sisdep1984/pdfs/Frey_26.pdf

Disclosing that heterostructure devices (HEMT, TEGFET, MODFET, etc.) should be treatable as logical extensions since the dimensions of the regions are small enough that quantum effects should be considered (Section 6.2 on Page 346).

The following classes and subclasses were searched:

Class 117 (Single-crystal, Oriented-crystal, And Epitaxy Growth Processes; Non-coating Apparatus Therefor)

Subs. 105

Class 148 (Metal Treatment)

Subs. 174, 175, DIG174

Class 216 (Etching A Substrate: Processes)

Subs. 3

Class 257 (Active Solid-state Devices (e.g., Transistors, Solid-state Diodes))

Subs. 13, 14, 15, 192, 194, 197, 20, 23, 24, 25, 27, 9

Class 307 (Electrical Transmission Or Interconnection Systems)

Subs. 440, 445, 448, 450

Class 324 (Electricity: Measuring And Testing)

Subs. 678

Class 326 (Electronic Digital Logic Circuitry)

Subs. 132, 134, 2-5, 7

Class 327 (Miscellaneous Active Electrical Nonlinear Devices, Circuits, And Systems)

Subs. 169, 195, 326, 420, 499, 570

Class 365 (Static Information Storage And Retrieval)

Subs. 149

Class 377 (Electrical Pulse Counters, Pulse Dividers, Or Shift Registers: Circuits

And Systems)

Subs. 63

Class 438 (Semiconductor Device Manufacturing: Process)

Subs. 223, 224, 227, 228

Class 716 (Computer-aided Design And Analysis Of Circuits And Semiconductor Masks)

Subs. 1, 19

The following IPC-8 class and subclasses were searched:

Class H01L (SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR)

21/02 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of semiconductor devices or of parts thereof

21/203 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of semiconductor devices or of parts thereof; the devices having at least one potential-jump barrier or surface barrier, e.g. PN junction, depletion layer, carrier concentration layer; the devices having semiconductor bodies comprising elements of group IV of the Periodic System or $A_{III}B_V$ compounds with or without impurities, e.g. doping materials; Deposition of semiconductor materials on a substrate, e.g. epitaxial growth; using physical deposition, e.g. vacuum deposition, sputtering

21/331 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of semiconductor devices or of parts thereof; the devices having at least one potential-jump barrier or surface barrier, e.g. PN junction, depletion layer, carrier concentration layer; the devices having semiconductor bodies comprising elements of group IV of the Periodic System or $A_{III}B_V$ compounds with or without impurities, e.g. doping materials; Multistep processes for the manufacture of devices of the bipolar type, e.g. diodes, transistors, thyristors; the devices comprising three or more electrodes; Transistors

21/338 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of semiconductor devices or of parts thereof; the devices having at least one potential-jump barrier or surface barrier, e.g. PN junction, depletion layer, carrier concentration layer; the devices having semiconductor bodies comprising elements of group IV of the Periodic System or $A_{III}B_V$ compounds with or without impurities, e.g. doping materials; Multistep processes for the manufacture of devices of the unipolar type; Field-effect transistors; with a Schottky gate

21/363 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts

thereof; Manufacture or treatment of semiconductor devices or of parts thereof; the devices having at least one potential-jump barrier or surface barrier, e.g. PN junction, depletion layer, carrier concentration layer; the devices having semiconductor bodies not provided for in groups H01L 21/06, H01L 21/16, and H01L 21/18 with or without impurities, e.g. doping materials; Deposition of semiconductor materials on a substrate, e.g. epitaxial growth; using physical deposition, e.g. vacuum deposition, sputtering

- 21/70 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in or on a common substrate or of specific parts thereof; Manufacture of integrated circuit devices or of specific parts thereof
- 21/822 Processes or apparatus specially adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof; Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in or on a common substrate or of specific parts thereof; Manufacture of integrated circuit devices or of specific parts thereof; Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in, or on, a common substrate; with subsequent division of the substrate into plural individual devices; to produce devices, e.g. integrated circuits, each consisting of a plurality of components; the substrate being a semiconductor, using silicon technology
- 27/04 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate; including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier; the substrate being a semiconductor body
- 27/06 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate; including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier; the substrate being a semiconductor body; including a plurality of individual components in a non-repetitive configuration
- 29/02 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies
- 29/06 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump

barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by their shape; characterised by the shapes, relative sizes, or dispositions of the semiconductor regions

- 29/12 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by the materials of which they are formed
- 29/15 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by the materials of which they are formed; Structures with periodic or quasi periodic potential variation, e.g. multiple quantum wells, superlattices
- 29/165 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by the materials of which they are formed; including, apart from doping materials or other impurities, only elements of Group IV of the Periodic System in uncombined form; including two or more of the elements provided for in group H01L 29/16; in different semiconductor regions
- 29/205 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by the materials of which they are formed; including, apart from doping materials or other impurities, only $A_{III}B_V$ compounds; including two or more compounds; in different semiconductor regions
- 29/32 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Semiconductor bodies; characterised by physical imperfections; having polished or

roughened surface; the imperfections being within the semiconductor body

- 29/40 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Electrodes
- 29/51 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Electrodes; characterised by the materials of which they are formed; Metal-insulator semiconductor electrodes; Insulating materials associated therewith
- 29/66 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device
- 29/68 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched
- 29/73 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Bipolar devices; Transistor-type devices, i.e. able to continuously respond to applied control signals; Bipolar junction transistors
- 29/76 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the

electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Unipolar devices

- 29/772 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Unipolar devices; Field-effect transistors
- 29/778 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Unipolar devices; Field-effect transistors; with two-dimensional charge carrier gas channel, e.g. HEMT
- 29/80 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Unipolar devices; Field-effect transistors; with field effect produced by a PN or other rectifying junction gate
- 29/812 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; Types of semiconductor device; controllable by only the electric current supplied, or only the electric potential applied, to an electrode which does not carry the current to be rectified, amplified, or switched; Unipolar devices; Field-effect transistors; with field effect produced by a PN or other rectifying junction gate; with a Schottky gate
- 29/88 Semiconductor devices specially adapted for rectifying, amplifying, oscillating or switching and having at least one potential-jump barrier or surface barrier; Capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN-junction depletion layer or carrier concentration layer; Details of semiconductor

bodies or of electrodes thereof; Types of semiconductor device; controllable only by variation of the electric current supplied, or only the electric potential applied, to one or more of the electrodes carrying the current to be rectified, amplified, oscillated, or switched; Diodes; Tunnel-effect diodes

33/00 Semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission; Processes or apparatus specially adapted for the manufacture or treatment thereof or of parts thereof; Details thereof

The following U.S. references for 'Quantum-Well Logic Using Self-Generated Potentials' were cited in the search:

5,032,877 [Bate]	4,969,018 [Reed]	4,912,531 [Reed et al]
4,620,206 [Ohta et al]	4,599,728 [Alavi et al]	4,589,115 [Burnham et al]
4,581,621 [Reed]	4,575,924 [Reed et al]	4,532,535 [Gerber et al]
4,503,447 [Iafrate et al]	4,439,782 [Holonyak]	4,393,481 [Owen et al]
4,389,612 [Simmonds et al]	4,353,081 [Allyn et al]	4,313,178 [Stern et al]
4,291,390 [Stern et al]	4,263,664 [Owen et al]	4,051,393 [Fulton]
3,936,677 [Fulton et al]	3,862,436 [George]	3,833,894 [Aviram et al]
3,636,371 [Quillier]	3,533,008 [Lee]	3,254,276 [Schwarz et al]
3,197,839 [Tiemann]	3,065,432 [Duncan]	

The following foreign references for 'Quantum-Well Logic Using Self-Generated Potentials' were also noted of interest:

JPS 5990978A [Yanase et al]	JPS 5967676A [Yanase et al]
GB 2107927A [Matsushima et al]	GB 1084565A [N/A]
EP 0034166A1 [Bozler et al]	

The following patents appear to be relevant:

- 4,969,018 - Quantum-well Logic Using Self-generated Potentials
- 4,599,728 - Multi-quantum Well Laser Emitting At 1.5 μm
- 4,589,115 - Wavelength Tuning Of Quantum Well Heterostructure Lasers Using An External Grating
- 4,532,535 - Electrically Reprogrammable Non Volatile Memory Cell Floating Gate Eeprom With Tunneling To Substrate Region
- 4,393,481 - Nonvolatile Static Random Access Memory System
- 4,389,612 - Apparatus For Reducing Low Frequency Noise In Dc Biased Squids
- 4,353,081 - Graded Bandgap Rectifying Semiconductor Devices
- 4,313,178 - Analog Solid State Memory
- 4,291,390 - Analog Solid State Memory
- 4,263,664 - Nonvolatile Static Random Access Memory System
- 4,051,393 - Current Switched Josephson Junction Memory And Logic Circuits
- 3,936,677 - Supercurrent Device For Controlling Mobile Flux Vortices
- 3,862,436 - Triangle Wave Generator Having Direct Tunnel Diode Switch Control

3,833,894 - Organic Memory Device
3,636,371 - Saw-tooth Voltage Wave Generator Including Ramp Voltage
Source Controlled By Dual Stable State Tunnel-diode
Switchable Periodically By A Gating Circuit
3,533,008 - Push-pull Tunnel Diode Amplifier
3,254,276 - Solid-state Translating Device With Barrier-layers Formed By
Thin Metal And Semiconductor Material
3,197,839 - Method Of Fabricating Semiconductor Devices
3,065,432 - Wide Range Tunnel Diode Oscillator
GB 2107927A - Avalanche Photodiode With Quantum Well Layer
GB 1084565A - Transistor Switching Circuit
EP 0034166A1 - Semiconductor Embedded Layer Technology

These patents are representative of the reference searched. Copies of the cited references are enclosed for your further review. For additional information on the cited references, please see the patent family, located on the CD results, for related patents and the legal status of cited patents. Please do not hesitate to contact me with any questions regarding this search.

Best Regards,
EXPRESS SEARCH

A handwritten signature in black ink, reading "Christopher H. Flagg". The signature is fluid and cursive, with the first name "Christopher" being more prominent and the last name "Flagg" following in a similar style.

Cristopher H. Flagg
President

CHF

Enclosure: References for 'Quantum-Well Logic Using Self-Generated Potentials' – 31 Patents and 5 NPL References
Ref: E00-40002